
**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

ATTY.'S DOCKET: 2001 P 11904 US

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| Applicant.: Lee et al. | ) | Examiner: Not Yet Assigned |
| Serial No.: Not Yet Assigned | ) | Art Unit: Not Yet Assigned |
| Filed: November 19, 2001 | ) | |
| Title: FORMATION OF DUAL WORK FUNCTION GATE ELECTRODE | ) | |

**INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97 AND 1.98**

Honorable Commissioner of Patents and Trademarks
Box Patent Applications
Washington, D.C. 20231

Sir:

It is respectfully requested that the citations listed below be considered by the Patent and Trademark Office and made of official record in the above-identified application.

In the opinion of the undersigned, the below-listed citations represents the closest art known to the undersigned during the preparation of the above-identified application. This citation may be material to the examination of the subject application and is therefore submitted in compliance with the duty of disclosure defined in 37 C.F.R.§ 1.56 and 1.97.

A concise explanation of the relevance of the pertinent listed citations are set forth below.

## CONCISE EXPLANATION OF THE RELEVANCE OF THE PERTINENT LISTED CITATIONS

U.S. Patent 6,221,744 B1 is deemed pertinent for its disclosure of a method for forming a gate on a substrate during manufacturing of a semiconductor device. The process comprises:

forming a gate oxide layer on the substrate;

forming a polysilicon layer on the gate oxide layer;

forming an amorphous silicon layer on the polysilicon layer, wherein the amorphous silicon layer includes grains defining a plurality of first sizes;

defining the amorphous silicon layer and the polysilicon layer to form a gate structure; and

converting a first part of the grains of the amorphous silicon layer to polysilicon grains defining a plurality of second sizes so as to form a grain boundary between the amorphous silicon layer and the polysilicon layer, wherein each second size is smaller than the first size of the amorphous silicon layer grain.

U.S. Patent 6,159,810 is deemed pertinent for its disclosure of a gate and field effect transistors including amorphous impurity layers disclosed in these gate electrodes for integrated circuit field effect transistors are fabricated by forming a polysilicon layer on a gate insulating layer, forming an amorphous impurity layer on the polysilicon layer, and forming an amorphous silicon layer on the amorphous impurity layer.

More specifically, a polysilicon layer 15 is formed on the gate insulating layer 13. The polysilicon layer may be doped with an n-type impurity, such as arsenic or phosphorus, or a p-type impurity such as boron. In FIG. 4, an amorphous impurity layer 17 is formed on the polysilicon layer 15 . . . The amorphous impurity layer 17 may be formed using plasma

processing, ion implantation and/or other techniques. Then, as shown in FIG. 5, an amorphous silicon layer 19 is formed on the amorphous impurity layer 17 . . . Then, referring back to FIG. 2, the amorphous impurity layer 17 and the amorphous silicon layer 19 are converted into a polysilicon gate electrode having a first surface 201a adjacent the gate insulating layer 113, a second surface 201b opposite the gate insulating layer and a buried doped layer within the polysilicon gate electrode that is spaced apart from the first and second surfaces thereof. During this conversion, dopants in the amorphous impurity layer 117 may diffuse upward and downward into the polysilicon gate electrode 201, to form a doping profile that peaks within the polysilicon gate electrode 201." (col. 5, line 24-col. 6, line 4).

U.S. Patent 5,278,096 is deemed pertinent for its disclosure of a gate formation method with an undoped poly-silicon layer.

Formed upon polysilicon layer 15 is tungsten silicide layer 17 . . . Layer 17 is desirably formed by sputtering . . . The sputtering process produces a comparatively amorphous layer (col. 2, lines 18-27). Layer 19 is formed upon layer 17. Layer 19 may be any dielectric formed at a sufficiently low temperature to prevent crystallization of silicide layer 17 . . . Reference numeral 23 denotes an implantation species which may be, typically, elemental boron . . . [T]he peak of the implantation dosage is near the top surface of silicide layer 17 in the as-implanted stage. Little boron penetrates into polysilicon layer 15. After the implantation is performed, an annealing step, typically 30 minutes at approximately 900°C., is performed. The annealing step drives boron dopant from silicide 17 into polysilicon layer 15." (col. 2, line 33-col. 3, line 2).

U.S. Patent 5,464,789 is deemed pertinent for its disclosure of a method of manufacturing a CMOS semiconductor device is disclosed in. The method includes: forming a polysilicon film

over a gate oxide film, forming a film of an amorphous material over the polysilicon film, and implanting boron atoms into the polysilicon film through the film of amorphous material.

This Disclosure Statement under 37 C.F.R. §1.56 and 1.97 is not construed to the effect that no other material information as defined in 37 C.F.R. § 1.56(c) exist, or that this citation constitutes prior art under U.S.C. § 102 and 103.

Respectfully submitted,

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| Form PTO-1449 (REV. 8-83) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE | ATTY. DOCKET NO. | SERIAL NO. |
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| **INFORMATION DISCLOSURE CITATION** *(Use several sheets if necessary)* **FORMATION OF DUAL WORK FUNCTION GATE ELECTRODE** | 2001 P 11904 US | Not Yet Assigned |
| | APPLICANT Lee et al. | EXAMINER Not Yet Assigned |
| | FILING DATE November 19, 2001 | GROUP Not Yet Assigned |

jc971 U.S. PTO 09/988183 11/19/01

**U. S. PATENT DOCUMENTS**

| Examiner INITIAL | REF | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB-CLASS | FILING DATE IF APPROPRIATE |
|---|---|---|---|---|---|---|---|
| | | 5,278,096 | Jan. 11, 1994 | Lee et al. | 437 | 162 | |
| | | 5,464,789 | Nov. 07, 1995 | Saito | 438 | 592 | |
| | | 6,159,810 | Dec. 12, 2000 | Yang | 438 | 301 | |
| | | 6,221,744 | Apr. 24, 2001 | Shih et al. | 438 | 585 | |
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**FOREIGN PATENT DOCUMENTS**

| | REF | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUB-CLASS | TRANSLATION YES | TRANSLATION NO |
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**OTHER DOCUMENTS** *(Including Author, Title, Date, Pertinent Pages, Etc.)*

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***EXAMINER:** Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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